



Winbond
Bus Termination Regulator
W83310U
W83310UG



W83310U Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1.		03/Mar.	0.5	N.A.	All versions before 0.5 are for internal use only
2.		04/Feb.	0.51	N.A.	Add the thermal data inside
3		05/Mar.	0.6	N.A	Update the package dimension data.
4		06/Jan.	0.7	N.A	Add pb-free part no:W83310UG

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LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

The W83310U is a linear regulator which provides achieves continuous 2.0 Amp bi-directional sinking and driving capability for DDR SDRAM bus terminator application. The chip simply implement a stable power supply which can track half of input power dynamically for bus terminator with a single chip; that is the chip integrates two power MOSFETs. There is no any external power device needed. The W83310U is promoted with TO252 power package. With W83310U design, a high integration, high performance, and cost-effective solution is promoted.

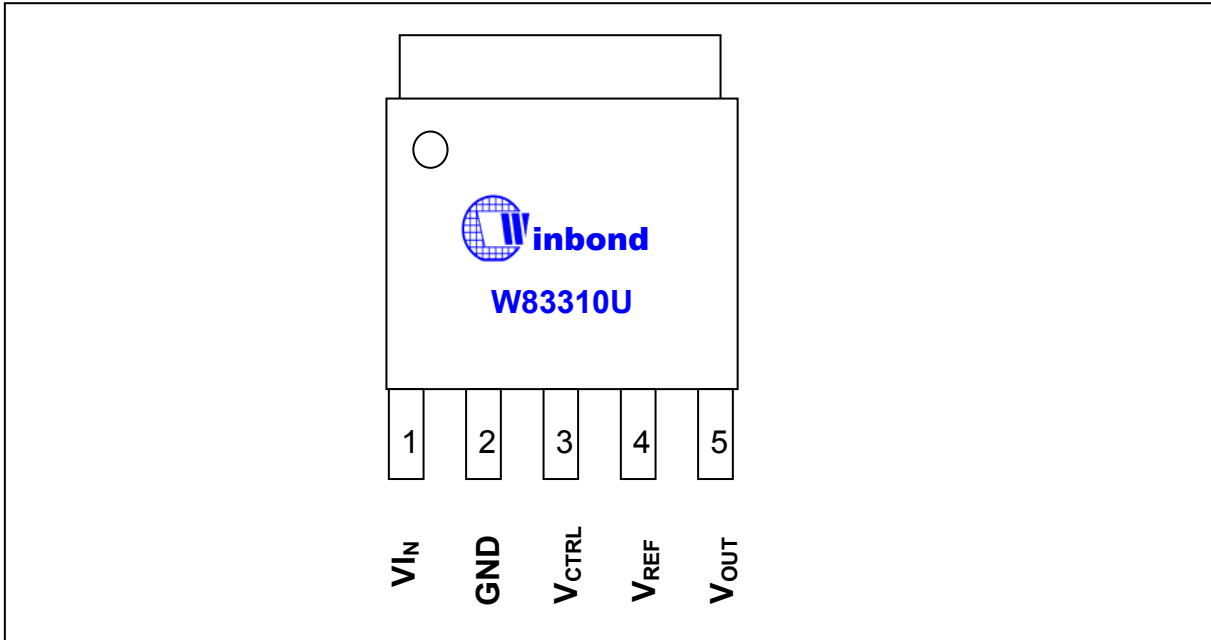
2. FEATURES

- Regulates a bi-directional power with driving and sinking capability
- Provides achieve continuous 2.0Amp driving and sinking current
- Power MOSFET integrated
- Low external component count
- Low output voltage offset
- Operates with +3.3V and +2.5V control power
- Power package TO252-5L
- Low cost and easy to use

3. APPLICATIONS

- DDR and DDR II Bus Termination Regulator
- Active Termination Bus
- SSTL-2
- SSTL-3

4. PIN CONFIGURATION AND DESCRIPTION

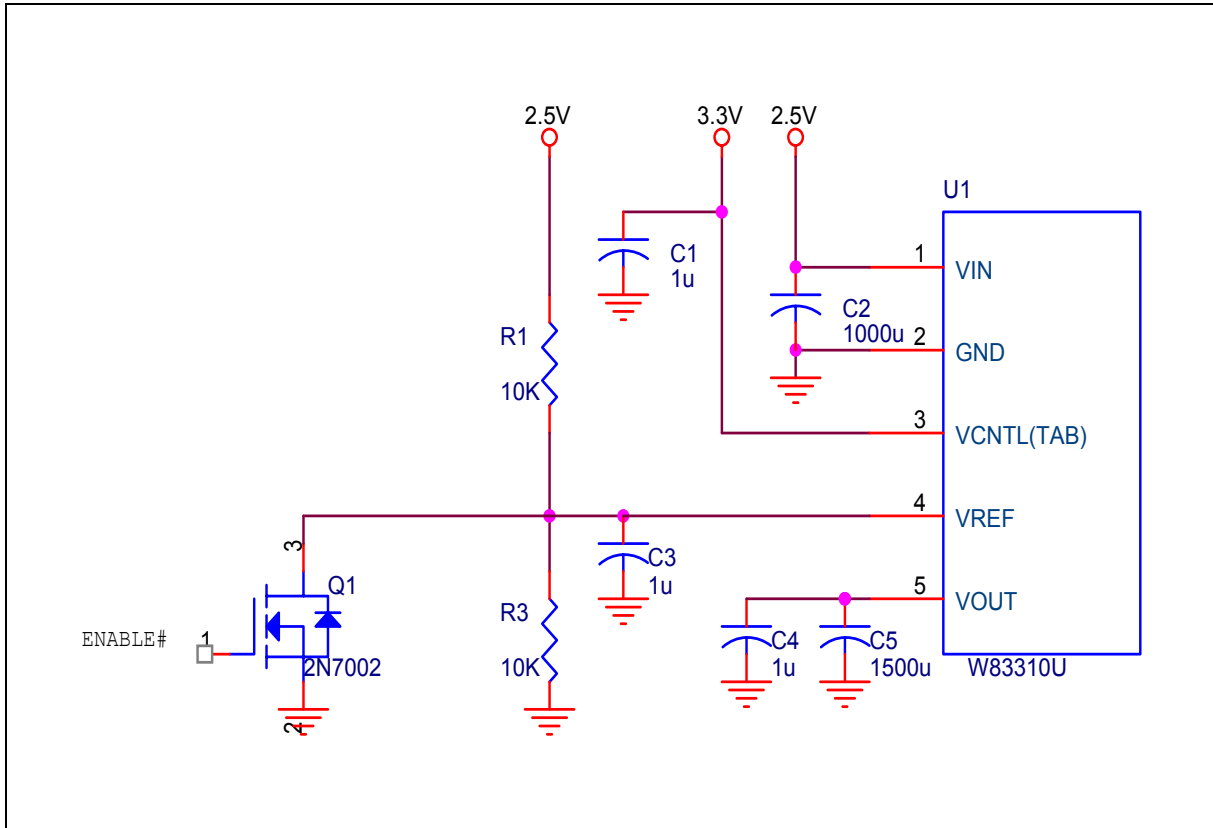


SYMBOL	PIN	FUNCTION
VIN	1	Power input pin.
GND	2	Ground.
VCNTL	3	Gate drive voltage.
VREF	4	Reference voltage and Chip enable.
VOUT	5	Output voltage.

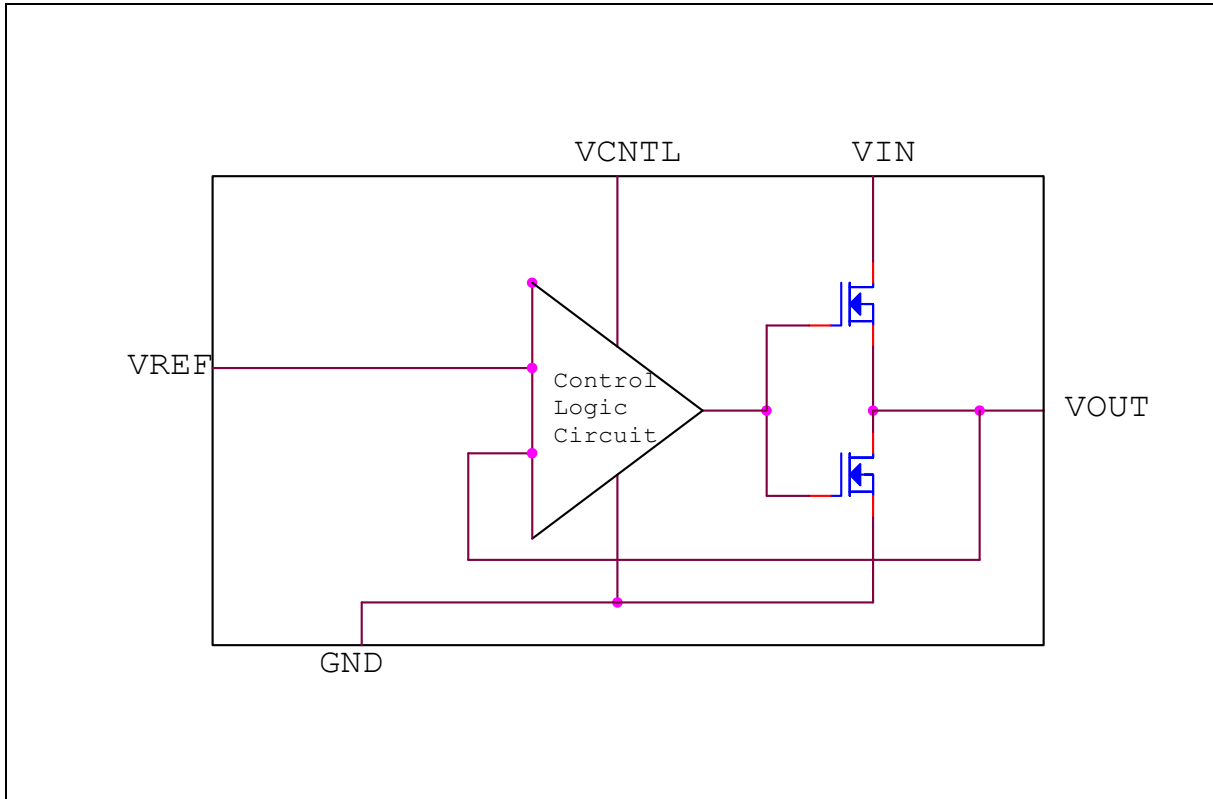
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5. APPLICATION CIRCUIT



6. INTERNAL BLOCK DIAGRAM - W83310U





7. ELECTRICAL CHARACTERISTICS

7.1 AC CHARACTERISTICS

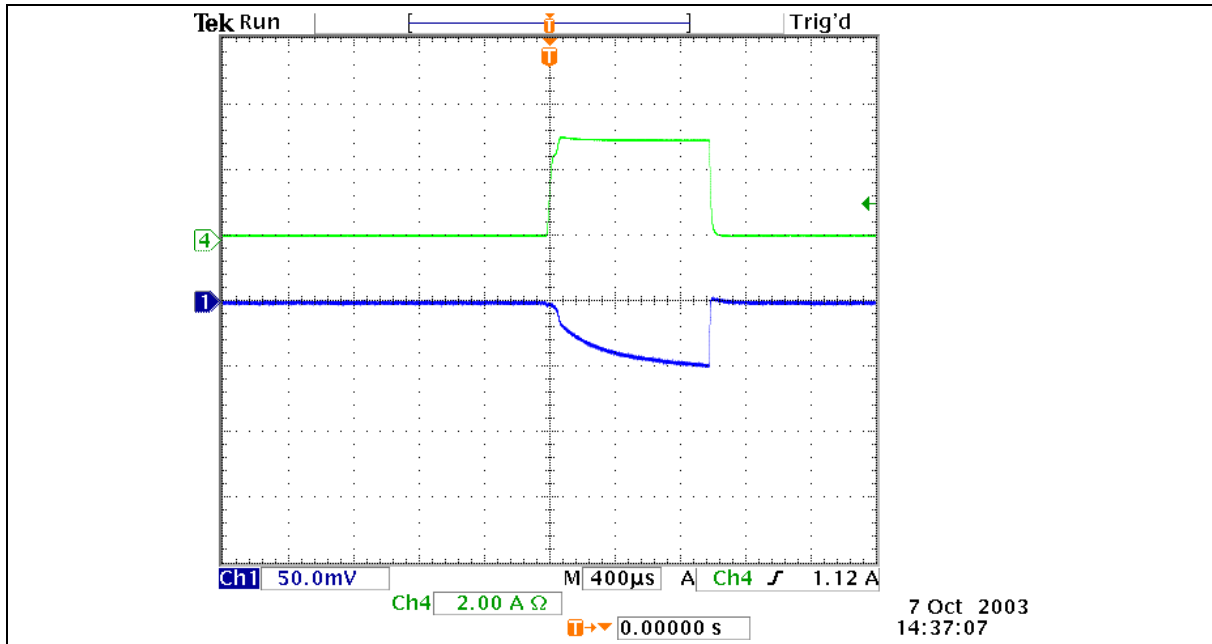
W83310U						
VIN=2.5V, VCNTL=3.3V, VREF=1.25V, Cout=100uF, TA = 0°C to +70°C						
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	TEST CONDITIONS
Output Offset Voltage	V _{OS}	-5	0	+5	mV	I _{OUT} =0A
Load Regulation			1.0		%	Loading: 0A→2.0A
			1.0			Loading: 0A→-2.0A
Input Voltage Range	V _{IN}	1.62	2.5	3.63	V	
	V _{CNTL}		3.3	3.63		
Operating Current of VCNTL	I _{CNTL}		0.5	1.0	mA	No Load(I _{OUT} =0A)
Shutdown Threshold Trigger		0.8			V	Output=High
				0.2	V	Output=Low
Shutdown Current	I _{SHDN}		10		uA	VREF<0.2V Loading=0.7A
Short Current Limit	I _{LMT}	4.0			A	

Note: Load regulation is tested with a 1ms duty pulse current and measuring V_{OUT}.

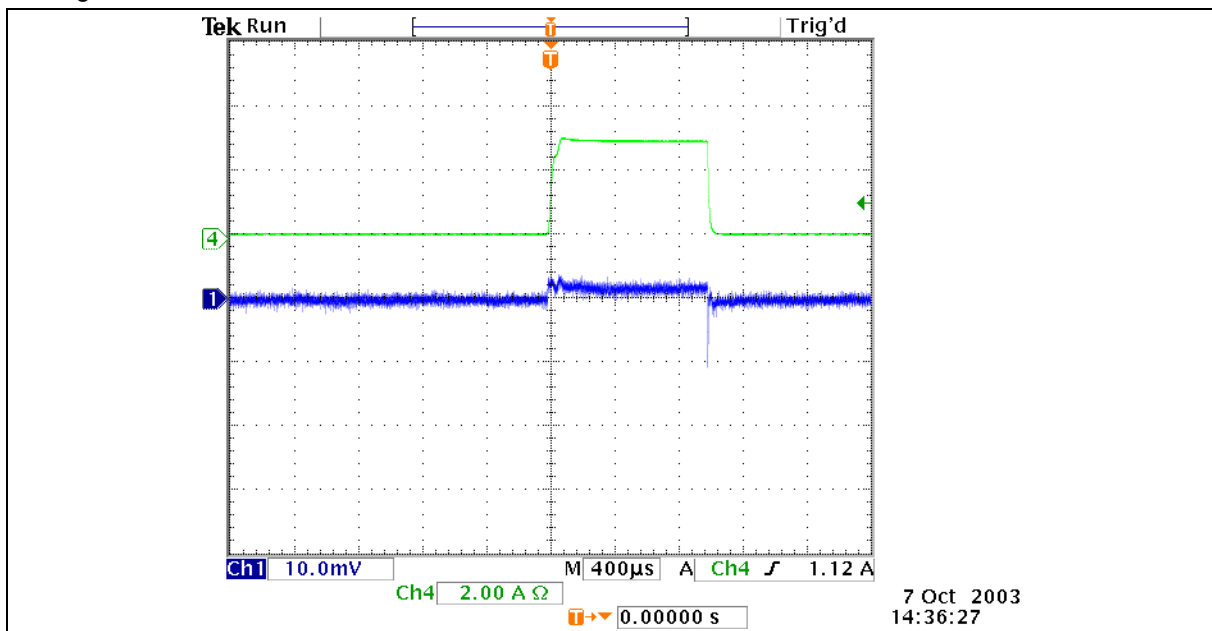


8. TYPICAL OPERATING WAVEFORM

-- Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 3.0Amp 1ms duty pulse driving current. $\Delta V \approx 50mV$.



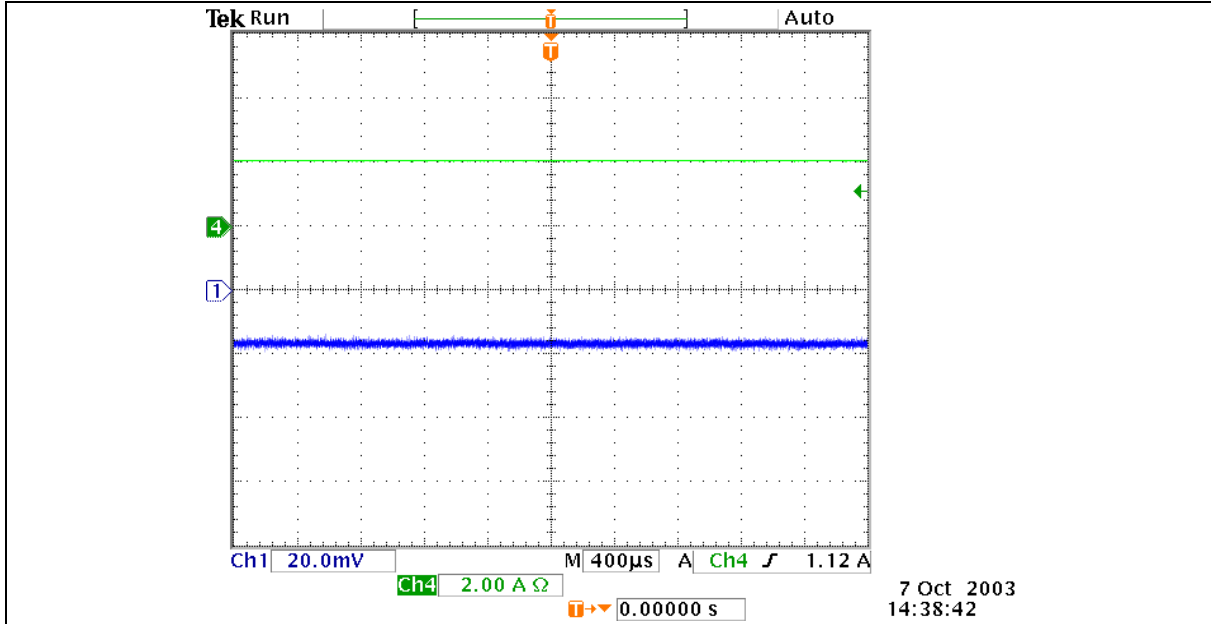
-- Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 3.0Amp 1ms duty pulse sinking current. $\Delta V \approx 5mV$.



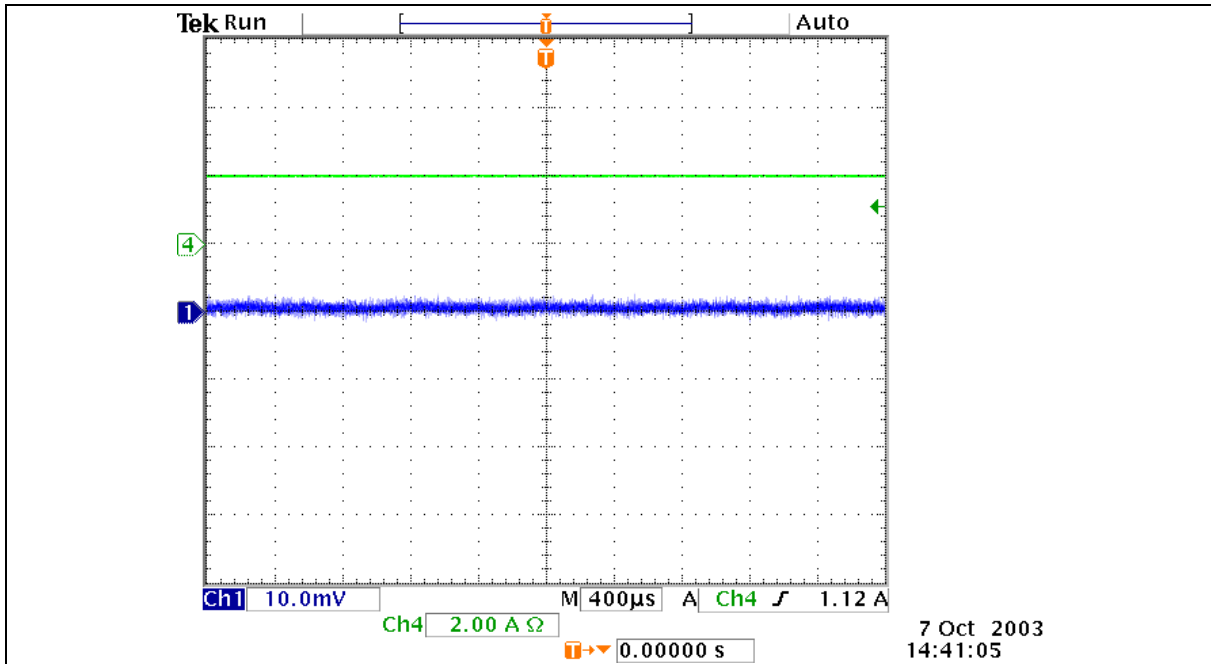
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-- Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 2.0Amp cont. driving current. $\Delta V \approx 20mV$.



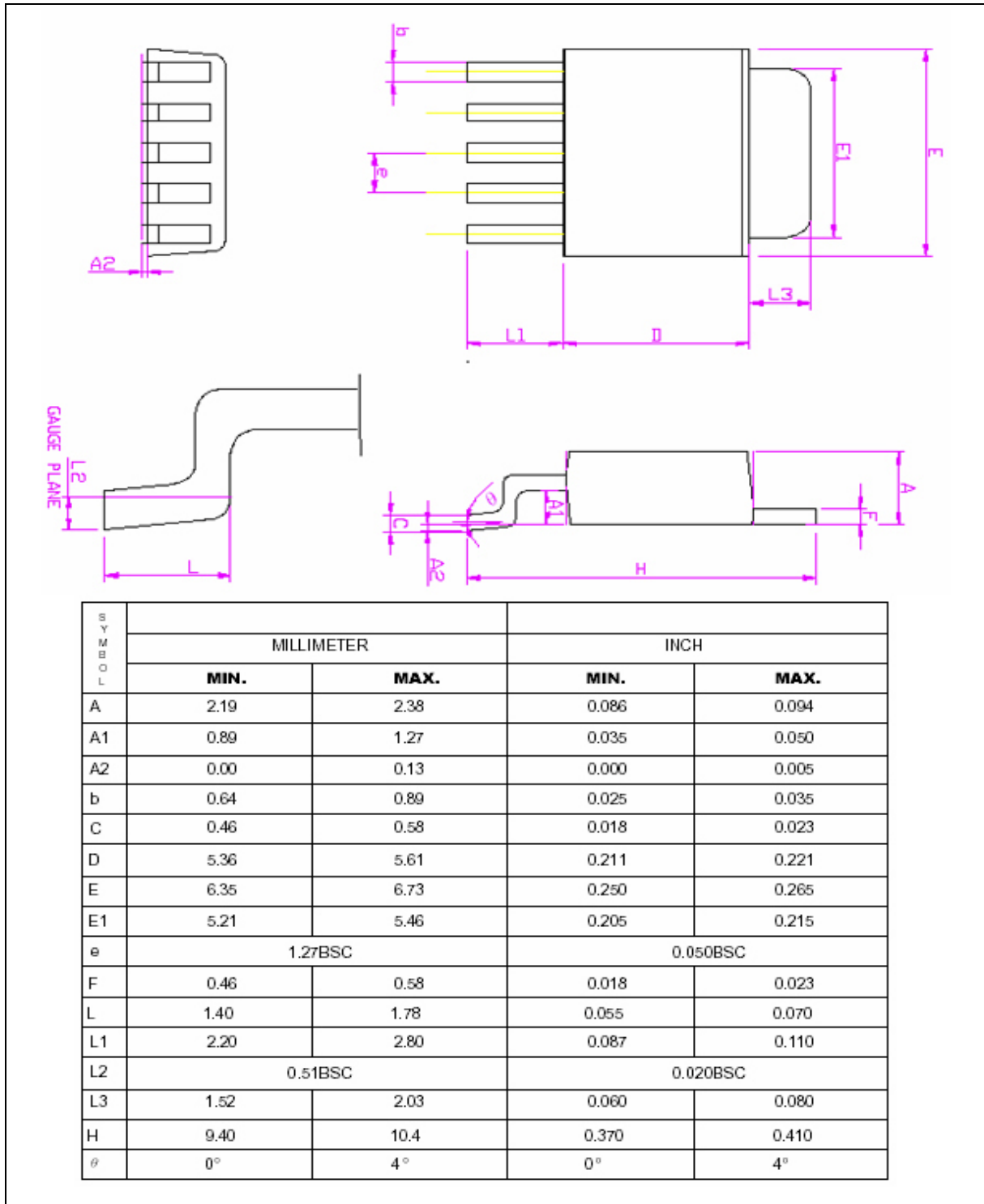
-- Load regulation with test condition - $V_{CTRL}=3.3V$; $V_{IN}=2.5V$; $V_{OUT}=1.25V$; 2.0Amp cont. sinking current. $\Delta V \approx 2mV$



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9. PACKAGE DIMENSION (TO252-5L)



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10. THERMAL PERFORMANCE

Test on Four-Layer (2S2P) JEDEC Test Board							
Package	Power (W)	Component Temp. (°C)					θ _{jc} (°C /W)
		Package	Die	Downset	Lead	Ambient	
TO-252-5L	3.18	96	145	79	78	25	15.5

11. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83310U	5L TO-252	

12. HOW TO READ THE TOP MARKING



Left line: Winbond logo

1st line: W83310U, W83310UG (Pb-free package) – the part number

2nd line: Tracking code Tracking code 316 G B

316: Packages assembled in Year 03rd, week 16

G: assembly house ID; O means OSE, G means GR, etc.

B: The IC version



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